FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11247-1E

MEMORY

8 M × 32 BIT HYPER PAGE MODE DRAM MODULE

MB8508E032BA-60

8 M × 32 Bit Hyper Page Mode DRAM Module, 5 V, 2-Bank

■ DESCRIPTION

The Fujitsu MB8508E032BA is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of sixteen MB8117405B devices. The MB8508E032BA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8508E032BA are the same as the MB8117405B which features hyper page mode operation providing extended valid time for data output and higher speed random access of up to 2,048 bits of data within the same row than the fast page mode. For ease of memory expansion, the MB8508E032BA is offered in a 72-pad Single In-line Memory Module package (SIMM).

■ PRODUCT LINE & FEATURES

Parameter		MB8508E032BA-60
$\overline{RAS}$ Access Time		60 ns max.
Random Cycle Time		104 ns min.
Address Access Time		30 ns max.
$\overline{CAS}$ Access Time		15 ns max.
Hyper Page Mode Cycle Time		25 ns min.
Power Dissipation	Operating Mode	4488 mW max.
	Standby Mode	88 mW (CMOS) / 176 mW (TTL)

- Organization : 8,388,608 words × 32 bits
- Memory : MB8117405B, 16 pcs
- 5.0V ±10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Hyper page mode operation (EDO)
- Package and Ordering Information:
  72-pin SIMM, order as
  MB8508E032BA-xxSG
  (SG = Gold Pad)
  MB8508E032BA-xxSS
  (SS = Solder Pad)

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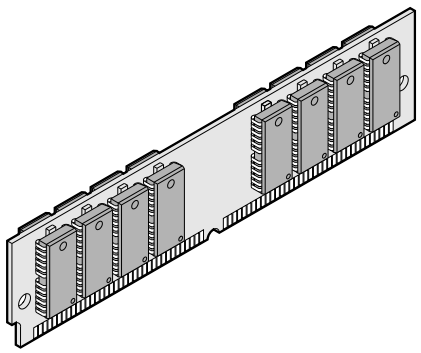
■ PACKAGE

72-pin plastic SIMM (socket type)



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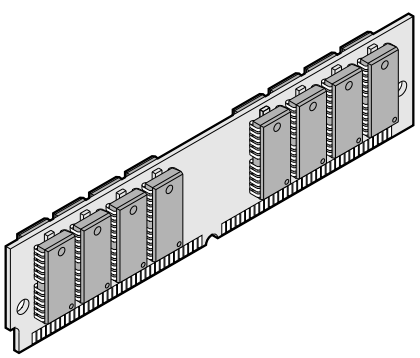

(MSS-72P-P80)

DQ_0	2	1	V_{SS}
DQ_1	4	3	DQ_{16}
DQ_2	6	5	DQ_{17}
DQ_3	8	7	DQ_{18}
V_{CC}	10	9	DQ_{19}
A_0	12	11	N.C.
A_2	14	13	A_1
A_4	16	15	A_3
A_6	18	17	A_5
DQ_4	20	19	A_{10}
DQ_5	22	21	DQ_{20}
DQ_6	24	23	DQ_{21}
DQ_7	26	25	DQ_{22}
A_7	28	27	DQ_{23}
V_{CC}	30	29	N.C.
A_9	32	31	A_8
$\overline{RAS}_2$	34	33	$\overline{RAS}_3$
N.C.	36	35	N.C.
N.C.	38	37	N.C.
$\overline{CAS}_0$	40	39	V_{SS}
$\overline{CAS}_3$	42	41	$\overline{CAS}_2$
$\overline{RAS}_0$	44	43	$\overline{CAS}_1$
N.C.	46	45	$\overline{RAS}_1$
N.C.	48	47	$\overline{WE}$
DQ_{24}	50	49	DQ_8
DQ_{25}	52	51	DQ_9
DQ_{26}	54	53	DQ_{10}
DQ_{27}	56	55	DQ_{11}
DQ_{28}	58	57	DQ_{12}
DQ_{29}	60	59	V_{CC}
DQ_{30}	62	61	DQ_{13}
DQ_{31}	64	63	DQ_{14}
N.C.	66	65	DQ_{15}
PD_2	68	67	PD_1
PD_4	70	69	PD_3
V_{SS}	72	71	N.C.

Pin #	Symbol	-60
67	PD_1	N.C.
68	PD_2	V_{SS}
69	PD_3	N.C.
70	PD_4	N.C.

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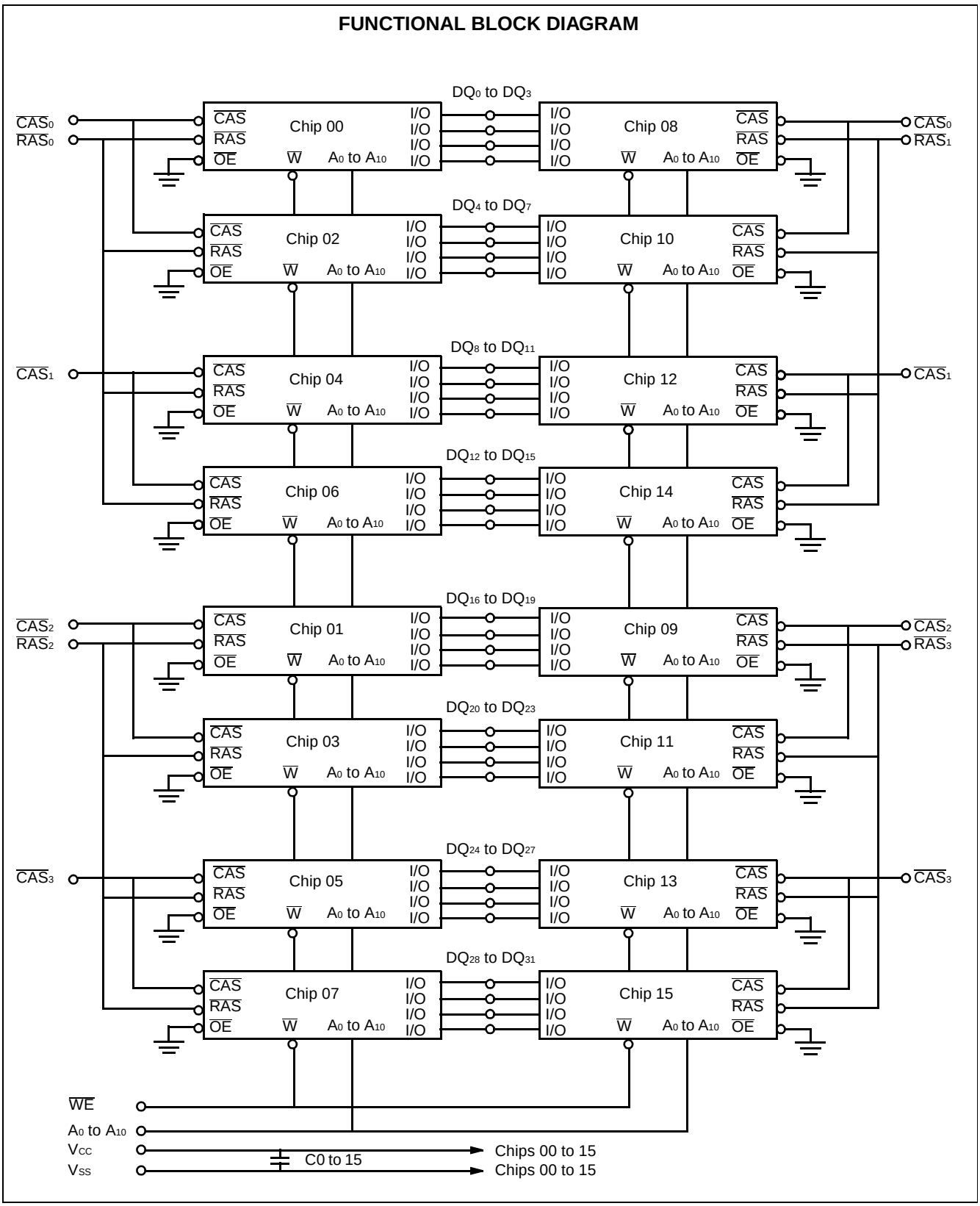
■ FUNCTIONAL BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	–50 to +50	mA
Power Dissipation	P_D	16	W
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITION

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, All Inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 10 ns are acceptable.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{CC} = 5.0 V)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_{10}	C_{IN1}	—	113	pF
Input Capacitance, $\overline{RAS}_0$ and $\overline{RAS}_3$	C_{IN2}	—	39	pF
Input Capacitance, $\overline{CAS}_0$ to $\overline{CAS}_3$	C_{IN3}	—	34	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	107	pF
I/O Capacitance, (DQ_0 to DQ_{31})	C_{DQ}	—	18	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value		Unit
					Min.	Max.	
Output High Voltage	*1		V_{OH}	I_{OH} = –5.0 mA	2.4	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = 4.2 mA	—	0.4	V
Input Leakage Current		$\overline{RAS}$	$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC}, 4.5 V ≤ V_{CC} ≤ 5.5 V, V_{SS} = 0 V, All other pins not under test = 0 V	–30	30	µA
		$\overline{CAS}$			–30	30	
		Address, $\overline{WE}$			–90	90	
Output Leakage Current			$I_{O(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V, Data out disabled	–20	20	µA
Operating Current (Average Power Supply Current)	*2	MB8508E032BA-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min	—	816	mA
Standby Current (Power Supply Current)		TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	32	mA
		CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	16	
Refresh Current#1 (Average Power Supply Current)	*2	MB8508E032BA-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min	—	816	mA
Hyper Page Mode Current	*2	MB8508E032BA-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{HPC} = min	—	576	mA
Refresh Current#2 (Average Power Supply Current)	*2	MB8508E032BA-60	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min	—	816	mA

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3 V.
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC2} is specified during $\overline{RAS}$ = V_{IH} and V_{IL} > –0.3 V.

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■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8508E032BA-60		Unit
				Min.	Max.	
1	Time between Refresh		t_{REF}	—	32.8	ms
2	Random Read/Write Cycle Time		t_{RC}	104	—	ns
3	Access Time from $\overline{RAS}$	*4,7	t_{RAC}	—	60	ns
4	Access Time from $\overline{CAS}$	*5,7	t_{CAC}	—	15	ns
5	Column Address Access Time	*6,7	t_{AA}	—	30	ns
6	Output Hold Time		t_{OH}	3	—	ns
7	Output Hold Time from $\overline{CAS}$		t_{CHC}	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	ns
9	Output Buffer Turn Off Delay Time	*8	t_{OFF}	—	15	ns
10	Output Buffer Turn Off Delay Time from $\overline{RAS}$	*8	t_{OFR}	—	15	ns
11	Output Buffer Turn Off Delay Time from $\overline{WE}$	*8	t_{WEZ}	—	15	ns
12	Transition Time		t_T	1	50	ns
13	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	ns
14	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	ns
15	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	ns
16	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Delay Time	*9.10	t_{RCD}	14	45	ns
18	$\overline{CAS}$ Pulse Width		t_{CAS}	10	—	ns
19	$\overline{CAS}$ Hold Time		t_{CSH}	40	—	ns
20	$\overline{CAS}$ Precharge Time (Normal)	*15	t_{CPN}	10	—	ns
21	Row Address Setup Time		t_{ASR}	0	—	ns
22	Row Address Hold Time		t_{RAH}	10	—	ns
23	Column Address Setup Time		t_{ASC}	0	—	ns
24	Column Address Hold Time		t_{CAH}	10	—	ns
25	Column Address Hold Time from $\overline{RAS}$		t_{AR}	24	—	ns
26	$\overline{RAS}$ to Column Address Delay Time	*11	t_{RAD}	12	30	ns
27	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	ns
28	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	23	—	ns
29	Read Command Setup Time		t_{RCS}	0	—	ns
30	Read Command Hold Time Referenced to $\overline{RAS}$	*12	t_{RRH}	0	—	ns
31	Read Command Hold Time Referenced to $\overline{CAS}$	*12	t_{RCH}	0	—	ns
32	Write Command Setup Time	*13	t_{WCS}	0	—	0
33	Write Command Hold Time		t_{WCH}	10	—	10
34	Write Command Hold Time from $\overline{RAS}$		t_{WCR}	24	—	24
35	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	MB8508E032BA-60		Unit
				Min.	Max.	
36	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	ns
37	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	10	—	ns
38	DIN Setup Time		t_{DS}	0	—	ns
39	DIN Hold Time		t_{DH}	10	—	ns
40	Date Hold Time from $\overline{RAS}$		t_{DHR}	24	—	ns
41	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	5	—	ns
42	$\overline{CAS}$ Setup Time (C-B-R Refresh)		t_{CSR}	0	—	ns
43	$\overline{CAS}$ Hold Time (C-B-R Refresh)		t_{CHR}	10	—	ns
44	$\overline{WE}$ Setup Time from $\overline{RAS}$	*16	t_{WSR}	0	—	ns
45	$\overline{WE}$ Hold Time from $\overline{RAS}$	*16	t_{WHR}	10	—	ns
46	$\overline{RAS}$ to Data In Delay Time		t_{RDD}	15	—	ns
47	$\overline{CAS}$ to Data In Delay Time		t_{CDD}	15	—	ns
48	DIN to $\overline{CAS}$ Delay Time		t_{DZC}	0	—	ns
49	$\overline{WE}$ Precharge Time		t_{WPZ}	5	—	ns
50	$\overline{WE}$ to Data In Delay Time		t_{WED}	15	—	ns
51	Hyper Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	—	100000	ns
52	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	25	—	ns
53	Access Time from $\overline{CAS}$ Precharge	*7,14	t_{CPA}	—	35	ns
54	Hyper Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	ns
55	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	ns

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Notes: *1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$- before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

*2. AC characteristics assume t_T = 5 ns.

*3. V_{IH} (min) and V_{IL} (max) are reference levels for measureing the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).

*4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.

*5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}$- t_{CAC} - t_T, access time is t_{CAC}.

*6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \geq t_{AA}$ - t_{CAC} - t_T, access time is t_{AA}.

*7. Measured with a load equivalent to two TTL loads and 100 pF.

*8. t_{OFF}, t_{OFR} and t_{WEZ} are specified that output buffer change to high impedance state.

*9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*10. t_{RCD} (min) = t_{RAH} (min) + 2 t_T + t_{ASC} (min).

*11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*14. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).

*15. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*16. Assumes that test mode function.

*Source: See MB8117405B Data Sheet for details on the electricals.

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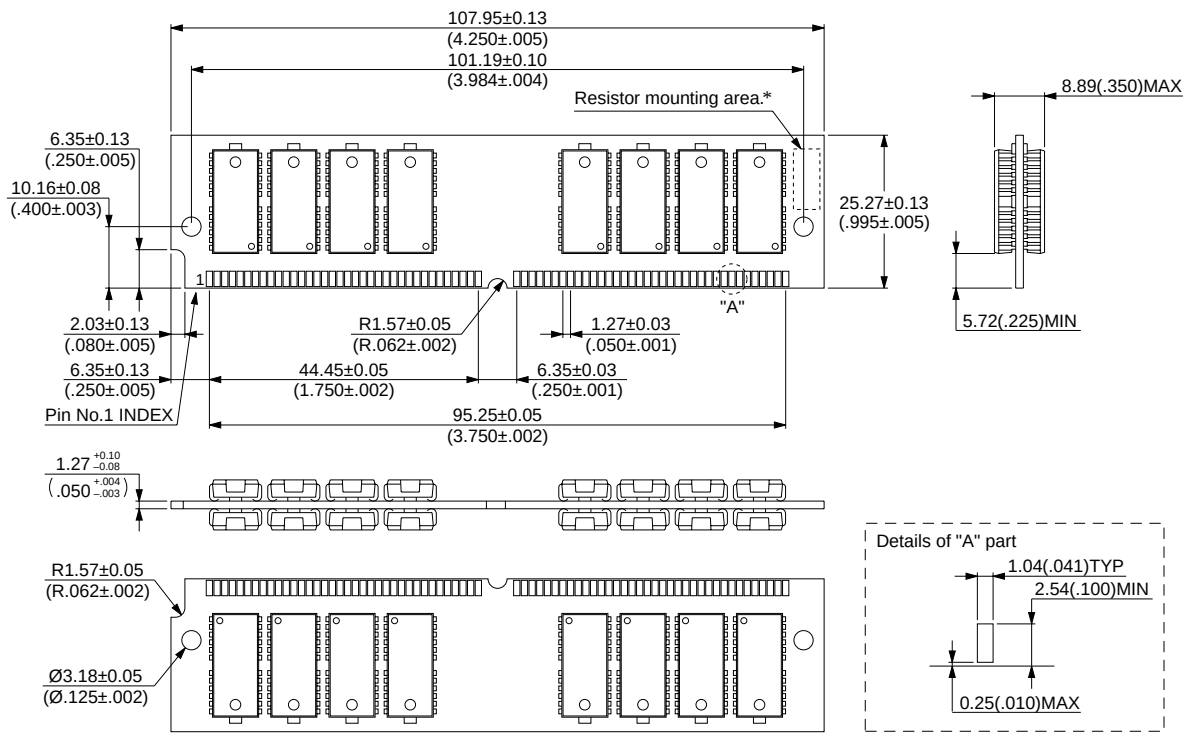
■ PACKAGE DIMENSIONS

72-pin plastic SIMM (socket type)
(MSS-72P-P78)

* : Resister thickness is 1.00 mm (.04 in.) maximum from board surface.



Dimension in mm (inches)

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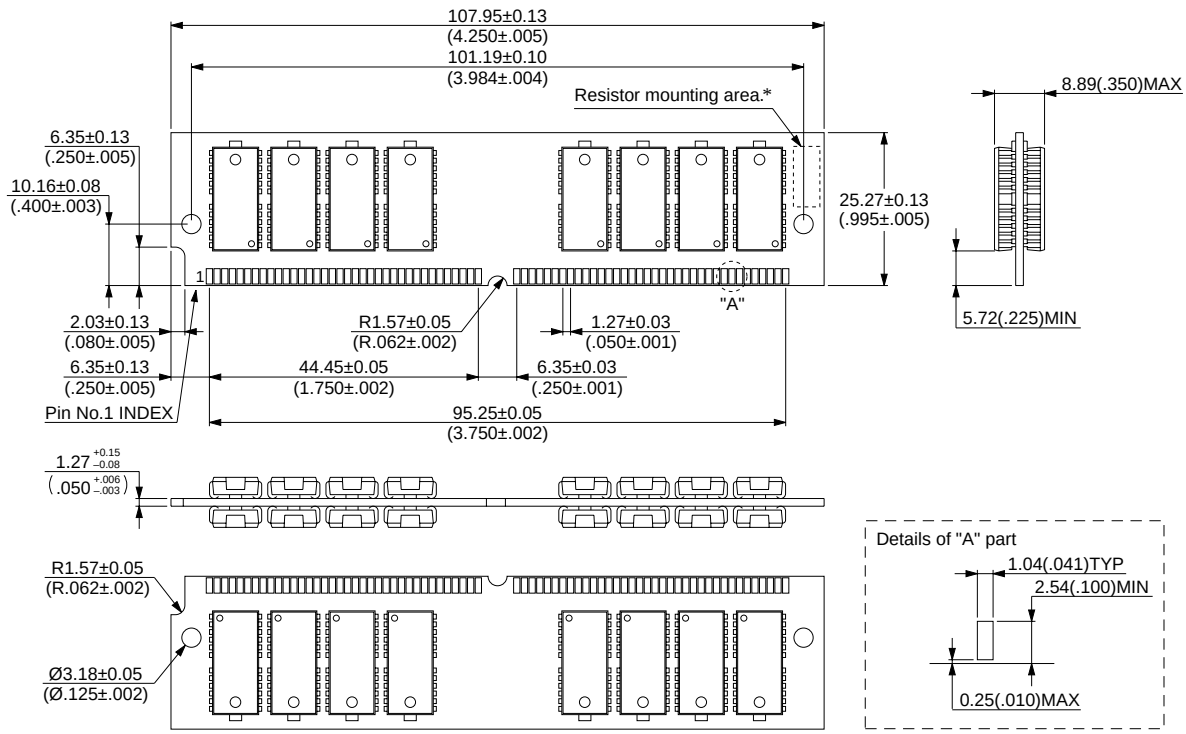
72-pin plastic SIMM (socket type)
(MSS-72P-P80)

* : Resister thickness is 1.00 mm (.04 in.) maximum from board surface.



Dimension in mm (inches)

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